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- **Título de la ponencia:**
  RISC-V for IoT, the PULP experience

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- **Abstract:**
  The Parallel Ultra Low Power (PULP) project was started in 2013 as a joint project between ETH Zurich and University of Bologna. From the beginning PULP was designed to be open source using a permissive license, and since 2015 embraced the RISC-V architecture. In this short time, this project has resulted in thirty seven ASIC tape-outs and widespread use in both academia and industry. In this talk, we will present the opportunities offered by open source hardware and RISC-V as well as challenges we have faced based on our work in running the PULP project.

- **Biografía:**
  Frank is the director of Microelectronics Design Center that supports IC, FPGA and PCB design within ETH Zurich and works as a Senior Scientist in the group of Luca Benini supporting him in running the group. He has been part of PULP project from its beginning. The Digital Circuits and Systems Group of ETH Zurich led by Prof. Luca Benini is working on energy efficient systems in a wide range of applications from IoT to HPC domain. In total, more than 60 people work in projects that cover system design, architectures, applications, and hardware design.